Claims 1, 2, 4-8 and 10-26 are pending in this application. Claims 1, 2, 4, 5 and 16-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. 5,331,184 (Kuwahara). Claims 6-8, 10-15 and 19-26 are withdrawn from consideration as directed to a non-elected species.

The claims have been amended only for clarity of the surfaces in which the various regions and layers are formed, and not in response to the prior art rejection.

Before addressing the prior art rejection, the Applicants would like to provide the following brief discussion of the invention. The present invention is directed to an electrode contact section incorporated into a semiconductor device. In such a semiconductor device, it is advantageous to reduce the resistance of the electrode contact section, especially in devices where the speed of turning off the device is important. However, in reducing the resistance of an electrode contact portion in such devices, it is necessary to increase the impurity concentration of the electrode contact portion. On the other hand, to increase the speed of turning off the device, it is necessary to reduce the impurity concentration of the electrode contract portion. Thus, the reducing the contact resistance and increasing the turnoff speed present a tradeoff. The present invention is directed to a device which can simultaneously achieve reduction of the contact resistance and avoid decreasing the turnoff speed.

As one example, as recited in claim 1, the thickness of an impurity layer in the contact section is not more than 1 μm and the thickness of a contact layer formed in the impurity layer is not more than 0.2 μm. The contact layer also has a higher impurity concentration than the impurity layer. The applicants have found that such contact structure can provide low contact resistance as well as good turnoff speed in the device.

Turning to the § 103 rejection, the Examiner describes how Kuwahara teaches a semiconductor device as shown in Fig. 2 having an anode layer 11 and anode regions 21 formed in the anode layer. The Office Action correctly finds that Kuwahara fails to teach a

device having the impurity layer and the contact layer of claim 1. As stated in column 3, lines 29-31, the device includes anode layer 11 having a thickness of 10-50 μm and, as stated in lines 45-48 of column 3, anode regions 21 formed in layer 11 have a thickness of 2 to 5 μm. These values are outside of the range of the values for the impurity layer and the contact layer recited in claims 1 and 16, and Kuwahara contains no suggestion of the contact structure of claim 1 or the device of claim 16.

The Office Action also states that Kuwahara discloses a contact layer of having a thickness at least 1/5 of the impurity layer. However, claims 1 and 16 do not recite a ratio but recite specific ranges of values of thickness of the impurity layer and contact layer. Kuwahara does not disclose layers with these thickness values. It follows that Kuwahara does not suggest a device or contact structure that can provide the aim of the contact structure of claim 1 and the device of claim 16.

The Office Action also refers to lines 10-19 of column 5 in Kuwahara describing reducing the thickness of the wafer. In particular, Kuwahara explains there that the wafer cost is increased in proportion to the thickness of the epitaxially grown layer. Kuwahara go on to further state that it is not necessary to increase the thickness of the epitaxial grown layer "considerably" because an IGBT having a breakdown voltage of 1,200V or more required for a thickness of about 100 μm can be realized in a lower cost than the conventional IGBT. Nothing in this portion of Kuwahara et al. describes reducing the thickness of impurity layer 11 to half that of the conventional thickness of the substrate. Nor does it suggest an impurity layer of no more than 1.0 μm thickness. In contrast, these lines describe reducing the cost of the wafer to be half that of the cost of the conventional IGBT and talk about a thickness of 100 μm. Nothing in this portion describes reducing the thickness of layer 11 to half of that of the conventional thickness of the substrate. Layer 11 is not mentioned.

Moreover, the substrate described in Kuwahara has a layer 11 of thickness 10-50 μm. Even reducing this by half would result in a thickness of 5-25 μm, which clearly does not suggest the device of claim 1 where the thickness of the impurity layer is 1 μm or less.

The impurity layer having a thickness of 1 μm or less and the contact layer having a thickness of 0.2 μm or less provides improved characteristics of the semiconductor device. These improvements are clearly not recognized in Kuwahara and thus clearly there is no suggestion of reducing the thickness of such layers to the values recited in claim 1 or claim 16.

As Kuwahara contains no suggestion for reducing the thickness of the impurity layer or the contact region to the values recited in claims 1 and 16, and the portion in column 5 does not support thinning of these layers, but instead describes reducing the cost of the wafer by half rather than the thickness of the wafer by half, there is no suggestion in Kuwahara of the device having the electrode contact section of claim 1 or the device of claim 16. Withdrawal of the §103 rejection is respectfully requested.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Finally, the attention of the Patent Office is directed to the change of address of Applicants' representative, effective January 6, 2003:

Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

1940 Duke Street

Alexandria, VA 22314.

Please direct all future communications to this new address.

Respectfully submitted,
OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Carl E. Schlier
Registration No. 34,426
Attorneys of Record

22850

703-413-3000
703-413-2220 Fax
GJM/CES/maj
I:\ATTY\CES\208546US.AM1.DOC

Marked-Up Copy
Serial No. 09/853,661
Amendment Filed: Herewith
02-26-03

IN THE SPECIFICATION

Please amend the paragraph at page 1, line 12 as follows:

In the prior art, [en] an electrode section incorporated in a semiconductor device is formed of an impurity layer provided in a semiconductor layer, and an electrode (made of, for example, a metal such as aluminum) that is in contact with the impurity layer. The impurity layer is often formed by ion implantation for the purpose of low cost.

Please amend the paragraph at page 3, line 14 as follows:

The present invention [has been] may [provided] provide an electrode contact section of a sufficiently low contact resistance even when forming an impurity layer by ion implantation. The invention [has been] may [provided] provide an electrode contact section in which the contact resistance and the carrier injection coefficient can simultaneously be reduced.

Please amend the paragraph at page 7, line 1 as follows:

As shown, a p-type impurity layer 2 is formed in an n-type semiconductor substrate 1. The n-type semiconductor layer 1 contains an n-type impurity such as [phosphor] phosphorus (P) with a substantially constant concentration of approx. 10^{14} ions/cm^3. The p-type impurity layer 2 is formed in a surface area of the semiconductor substrate 1 and contains a p-type impurity such as boron (B). The depth of the p-type impurity layer 2 from the surface of the semiconductor substrate 1 is set at 1.0 μm or less, for example, approx. 0.8 μm. Further, the

peak value of the concentration profile of the p-type impurity layer 2 is set at a value falling within the range of 10^{17} - 10^{18} ions/cm^3.

Please amend the paragraph at page 13, line 20 as follows:

In this example, a p-type impurity layer 2 is formed in an n-type semiconductor substrate 1. The n-type semiconductor layer 1 contains an n-type impurity such as [phosphor] phosphorus (P) with a substantially constant concentration of approx. 10^{14} ions /cm^3. The p-type impurity layer 2 is formed in a surface area of the semiconductor substrate 1 and contains a p-type impurity such as boron (B). The depth of the p-type impurity layer 2 from the surface of the semiconductor substrate 1 is set at 1.0 μm or less, for example, approx. 0.8 μm. Further, the peak value of the concentration profile of the p-type impurity layer 2 is set at a value falling within the range of 10^{17} - 10^{18} ions/cm^3.

Please amend the paragraph at page 52, line 4 as follows:

Subsequently, an n-type impurity such as [phosphor] phosphorus (P) is implanted into the other surface of the semiconductor substrate 1 by ion implantation, and subjected to a thermal diffusion treatment, thereby forming an n^+-type base layer 12 in a surface portion of the other surface of the semiconductor substrate 1.

Please amend the paragraph at page 59, line 1 as follows:

Subsequently, an n-type impurity such as [phosphor] phosphorus (P) is implanted into the other surface of the semiconductor substrate 1 by ion implantation, and subjected to a thermal diffusion treatment, thereby forming an n^+-type base layer 12 in a surface portion of the other surface of the semiconductor substrate 1.

IN THE CLAIMS

Please amend the claims as follows:

1. (Twice Amended) An electrode contact section incorporated in a semiconductor device, comprising:

a first-conductivity-type semiconductor substrate;

a second-conductivity-type impurity layer formed in one surface of the semiconductor substrate and having a thickness of not more than 1.0 μm from [a] the one surface of the semiconductor substrate;

a second-conductivity-type contact layer formed in the impurity layer and having a thickness of not more than 0.2 μm from the one surface of the semiconductor substrate, the contact layer being thinner than the impurity layer and having a higher impurity concentration than the impurity layer;

a first electrode formed on the contact layer; and

a second electrode formed at another surface [side] of the semiconductor substrate for allowing a current to flow between the first and second electrodes.

11. (Amended) The electrode contact section according to claim 7, wherein the impurity layer has a thickness of not more than 1.0 μm from [a] the one surface of the semiconductor substrate.

12. (Amended) The electrode contact section according to claim 7, wherein the contact layer has a thickness of not more than 0.2 μm from [a] the one surface of the semiconductor substrate.

13. (Twice Amended) The electrode contact section according to claim 7, wherein:

the silicide layer has a thickness of not more than 0.2 μm from [a] the one surface of the semiconductor substrate, and

the silicide layer is thinner than the contact layer.

16. (Amended) A semiconductor device comprising:

a first-conductivity-type semiconductor substrate;

a second-conductivity-type base region formed in [a] one surface of the semiconductor substrate;

a first-conductivity-type impurity region formed in the base region;

a first electrode connected to the first-conductivity-type impurity region;

a gate electrode connected to the base region via an insulation film;

a second-conductivity-type impurity region formed in [the] another surface of the semiconductor substrate and having a thickness of not more than 1.0 μm from the another surface of the semiconductor substrate;

a second-conductivity-type contact region formed in the second-conductivity-type impurity region and having a thickness of not more than 0.2 μm from the another surface of the semiconductor substrate, the contact region being thinner than the second-conductivity-type impurity region and having a higher impurity concentration than the second-conductivity-type impurity region; and

a second electrode formed on the contact region.

18. (Amended) The semiconductor device according to claim 16, wherein the second-conductivity-type impurity region is formed in the entire another surface of the semiconductor substrate.

19. (Amended) The semiconductor device according to claim 16, wherein the impurity region is formed in a portion less than the entire another surface of the semiconductor substrate.

20. (Amended) A semiconductor device comprising:

a first-conductivity-type semiconductor substrate;

a second-conductivity-type base region formed in [a] one surface of the semiconductor substrate;

a first-conductivity-type impurity region formed in the base region;

a first electrode connected to the first-conductivity-type impurity region;

a gate electrode connected to the base region via an insulation film;

a second-conductivity-type impurity region formed in [the] another surface of the semiconductor substrate;

a second-conductivity-type contact region formed in the impurity region, the second-conductivity-type contact region being thinner than the second-conductivity-type impurity region and having a higher impurity concentration than the second-conductivity-type impurity region;

a second electrode formed on the contact region; and

a silicide region formed between the second electrode and the contact region, the silicide region having a contact-region-side end thereof made to substantially correspond to that portion of the contact region at which a concentration profile of the contact region assumes a peak value.

22. (Amended) The semiconductor device according to claim 20, wherein the second-conductivity-type impurity region has a thickness of not more than 1.0 μm from the another surface of the semiconductor substrate.

23. (Amended) The semiconductor device according to claim 20, wherein the contact region has a thickness of not more than 0.2 μm from the another surface of the semiconductor substrate.

24. (Amended) The semiconductor device according to claim 20, wherein:

the silicide region has a thickness of not more than 0.2 μm from the another surface of the semiconductor substrate, and

the silicide layer is thinner than the contact region.

25. (Amended) The semiconductor device according to claim 20, wherein the second-conductivity-type impurity region is formed in the entire another surface of the semiconductor substrate.

26. (Amended) The semiconductor device according to claim 20, wherein the second-conductivity-type impurity region is formed in a portion less than the entire another surface of the semiconductor substrate.